

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY GURAJADA VIZIANAGARAM
IV B. Tech I Semester Advanced Supplementary Examinations March - 2025

DIGITAL IC DESIGN USING CMOS

(Electronics & Communication Engineering)

Time: 3 hours

Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from Each unit
 All Questions Carry Equal Marks

UNIT-I

1. Explain the following terms in detail [5+5+4
 (i) Transient response (ii) Rise time (iii) Fall time =14M]
 (OR)

2. a) What are the criteria for voltage threshold for high level and low level in NMOS inverter characteristics? Explain [7M]
 b) Write short notes on Pseudo NMOS logic gates [7M]

UNIT-II

3. Design and implement CMOS full adder circuit? Explain in detail. [14M]
 (OR)

4. a) Design and implement AOI and OIA using CMOS? [7M]
 b) Write short notes on transmission gates with the relevant circuits? [7M]

UNIT-III

5. a) Explain the concept of Behavior of bistable elements in detail. [7M]
 b) Write short notes on SR latch in sequential MOS logic? [7M]
 (OR)

6. a) Explain the operation of CMOS D latch along with diagram [7M]
 b) Write short notes on edge triggered flip-flop in detail? [7M]

UNIT-IV

7. a) Explain the concept of Voltage Bootstrapping along with example. [7M]
 b) Write short notes on Dynamic CMOS transmission gate logic in detail? [7M]
 (OR)

8. a) Explain the basic principle of Dynamic Logic Circuits in detail. [7M]
 b) Write short notes on dynamic pass transistor circuits in detail? [7M]

UNIT-V

9. a) Explain the principle of NOR gate flash memory with a neat diagram. [7M]
 b) Compare the SRAM and DRAM? [7M]
 (OR)

10. Explain the following terms in detail [5+5+4
 (i) Capacitive Parasitics (ii) Resistive Parasitics (iii) Inductive Parasitics =14M]
